FIG. 1A

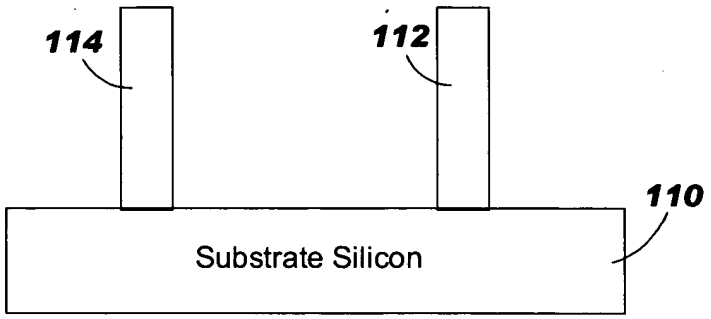


FIG. 1B

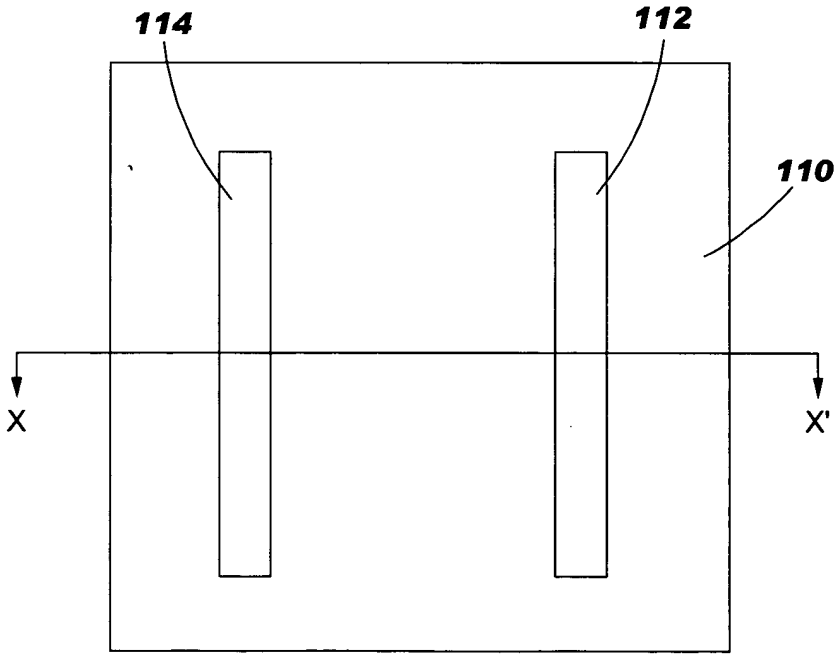


FIG. 2A

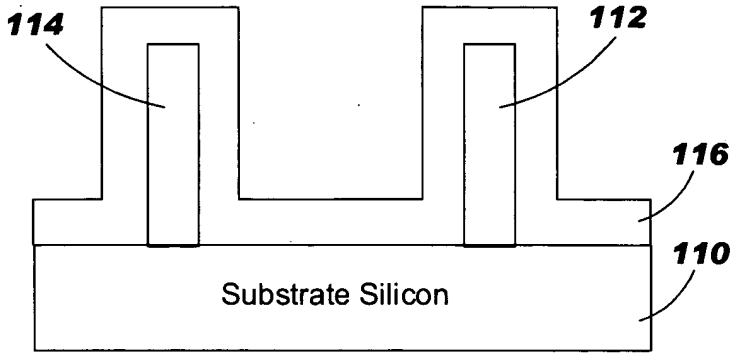


FIG. 2B

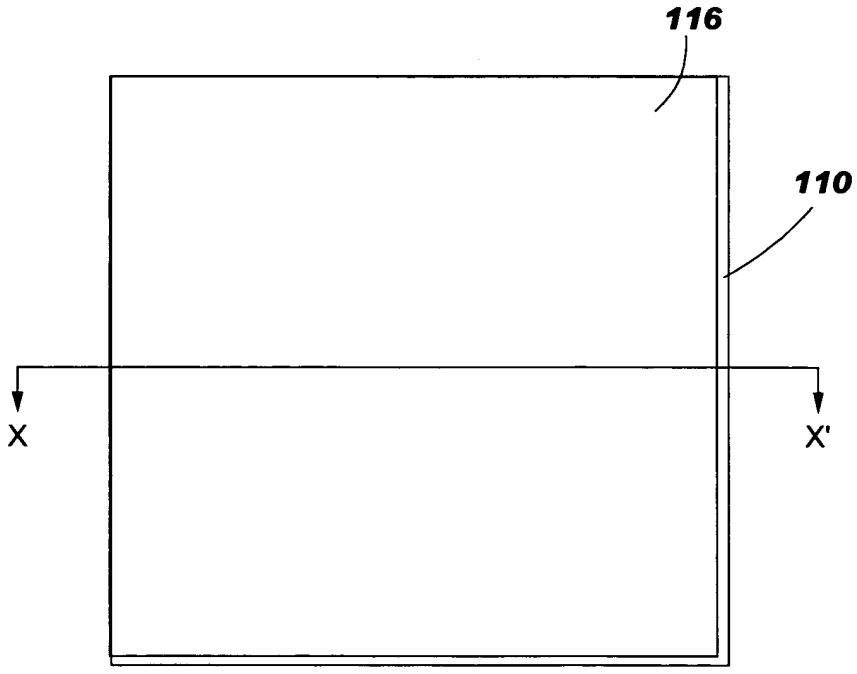


FIG. 3A

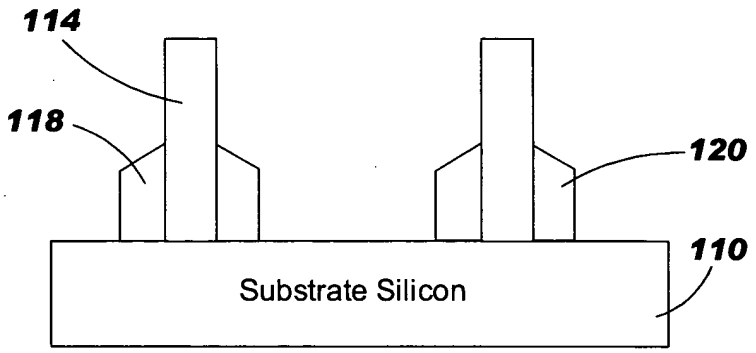


FIG. 3B

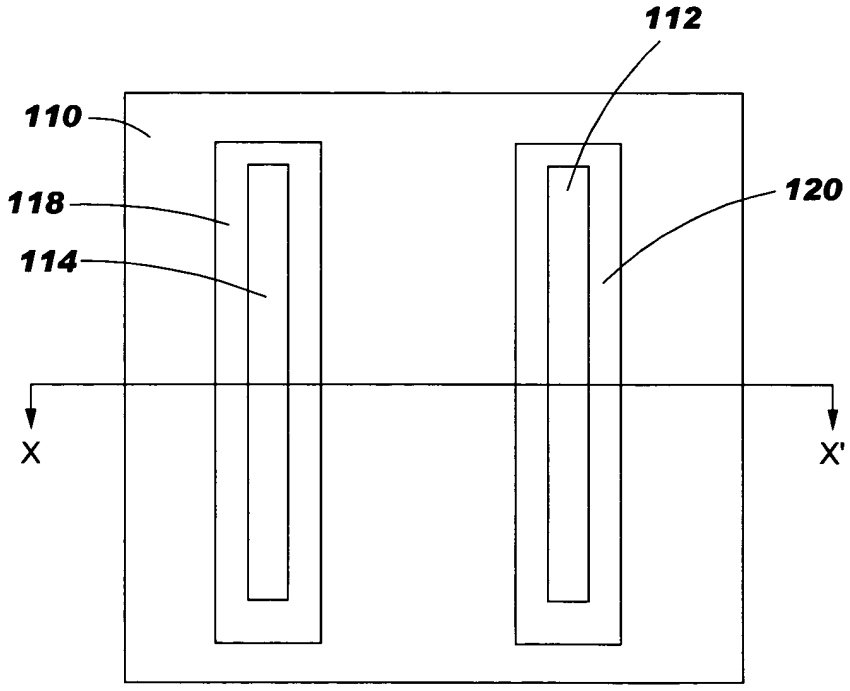


FIG. 4A

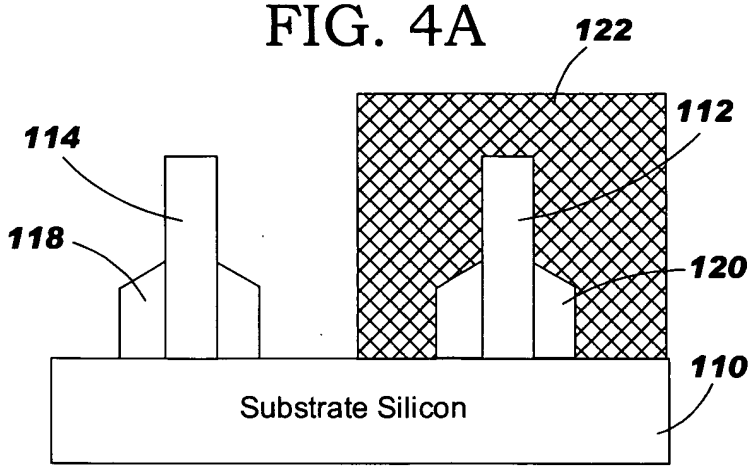


FIG. 4B

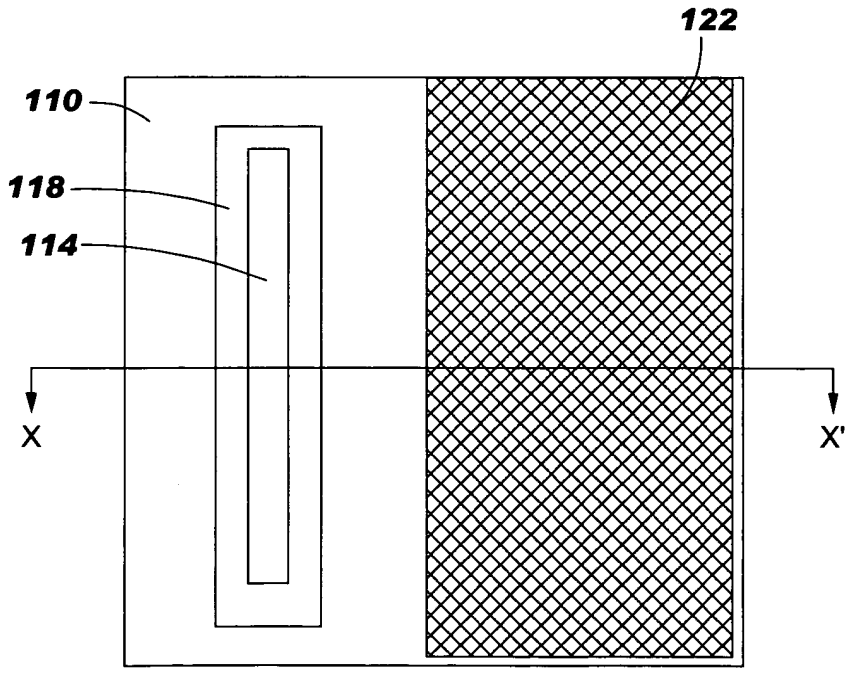


FIG. 5A

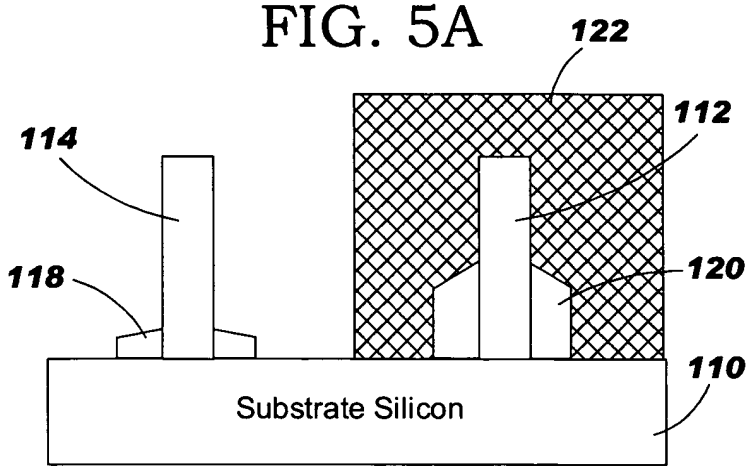


FIG. 5B

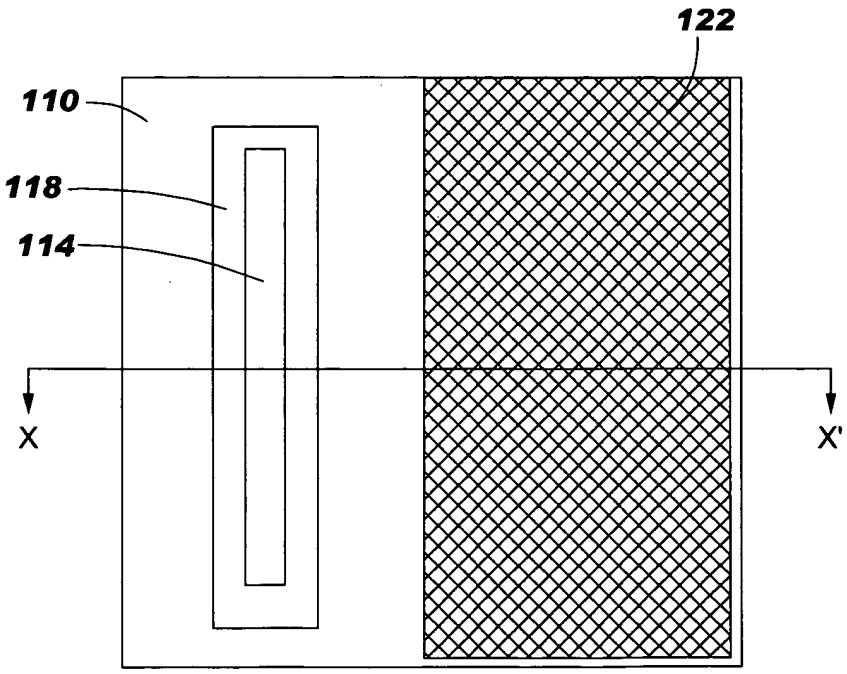


FIG. 6A

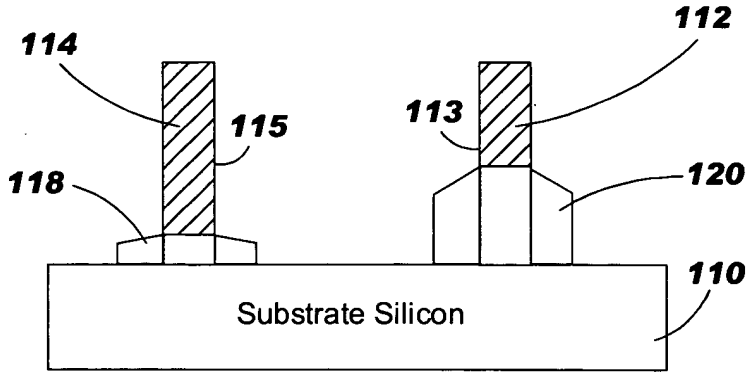

114
115
118
113
112
120
110
Substrate Silicon

FIG. 6B

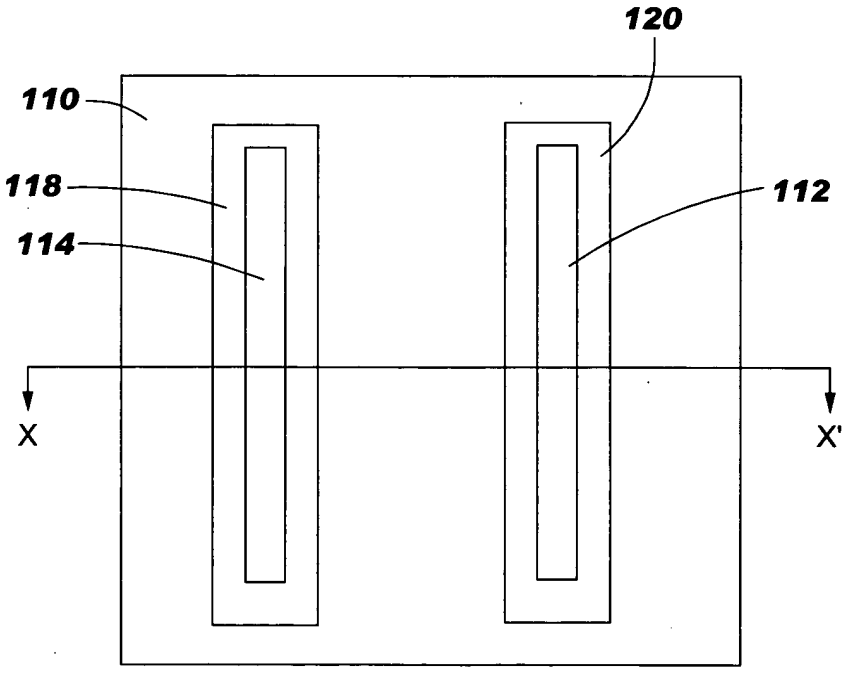

120
110
118
114
112
X
X'

FIG. 7A

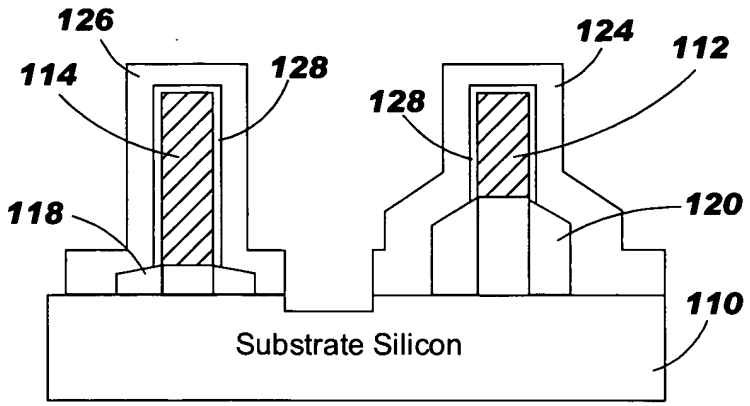

126
114
128
124
112
128
118
120
110
Substrate Silicon

FIG. 7B

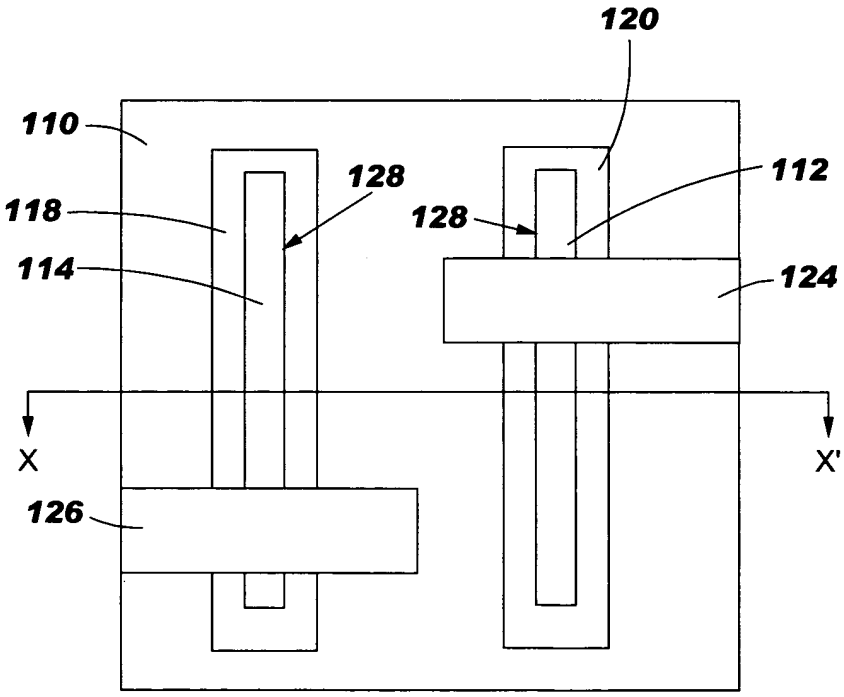

120
110
128
112
118
128
114
124
X
X'
126

FIG. 8A

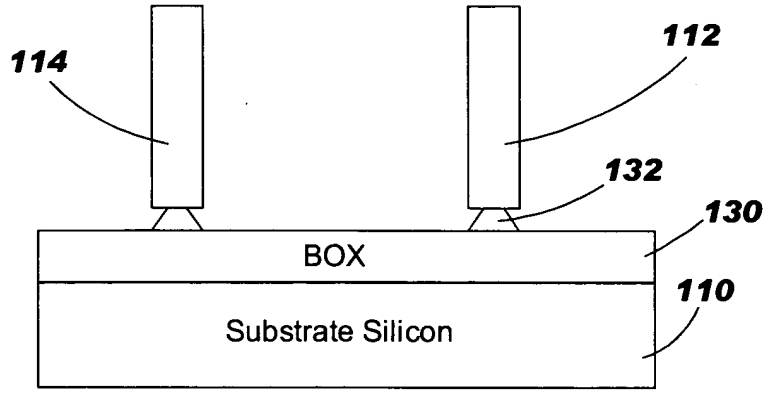


FIG. 8B

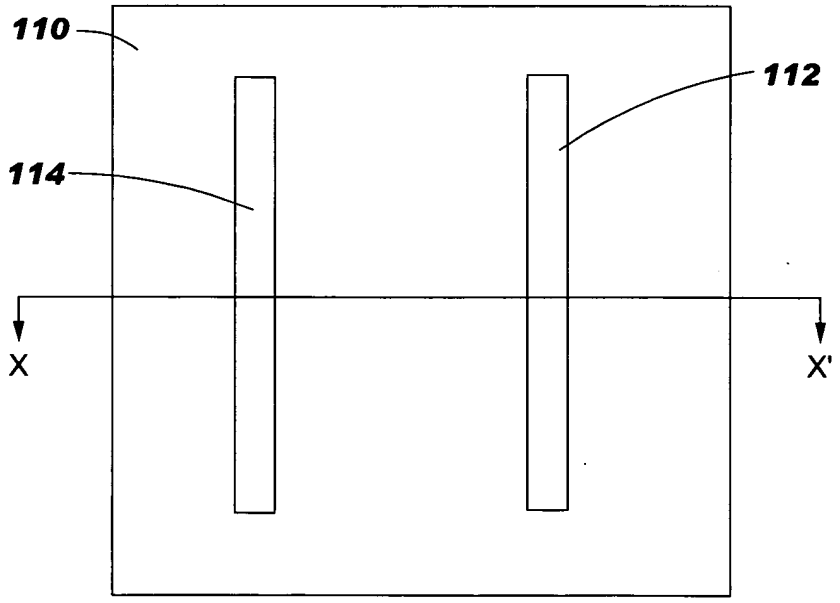


FIG. 9A

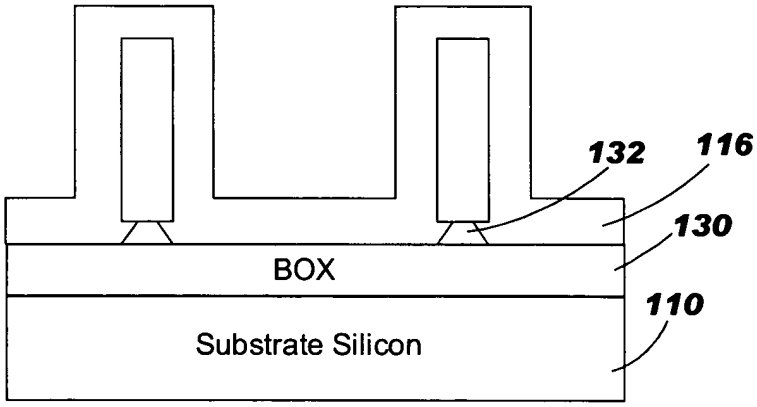


FIG. 9B

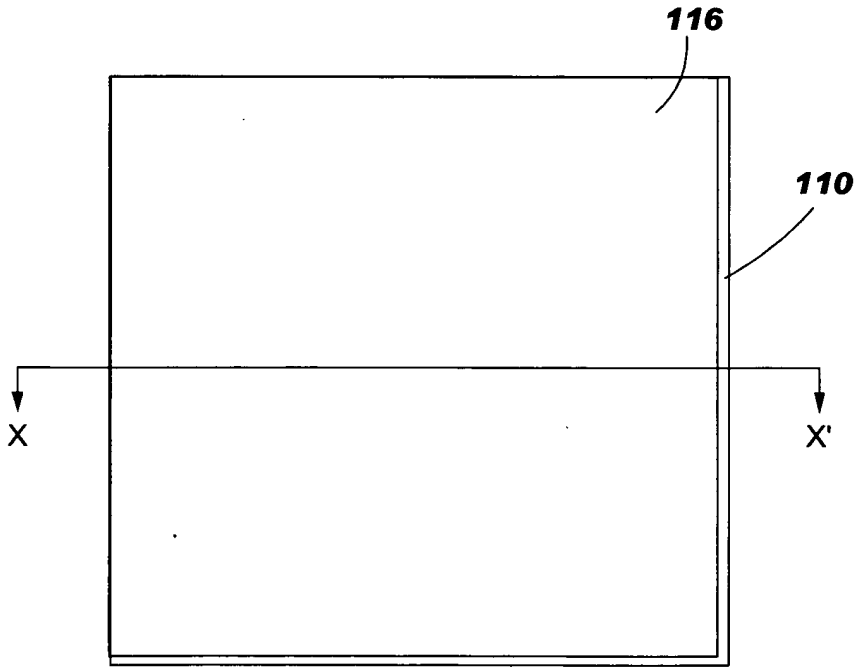


FIG. 10A

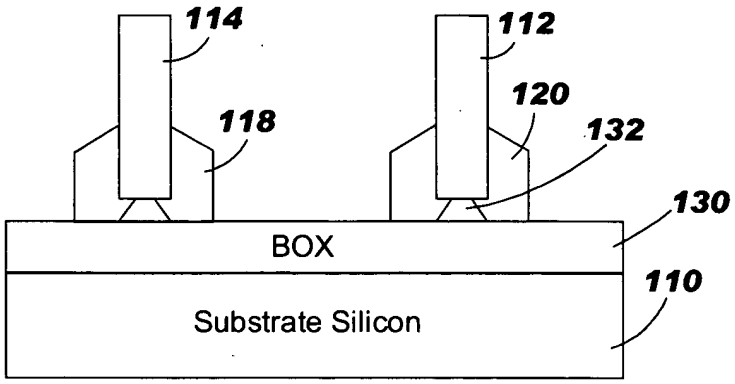


FIG. 10B

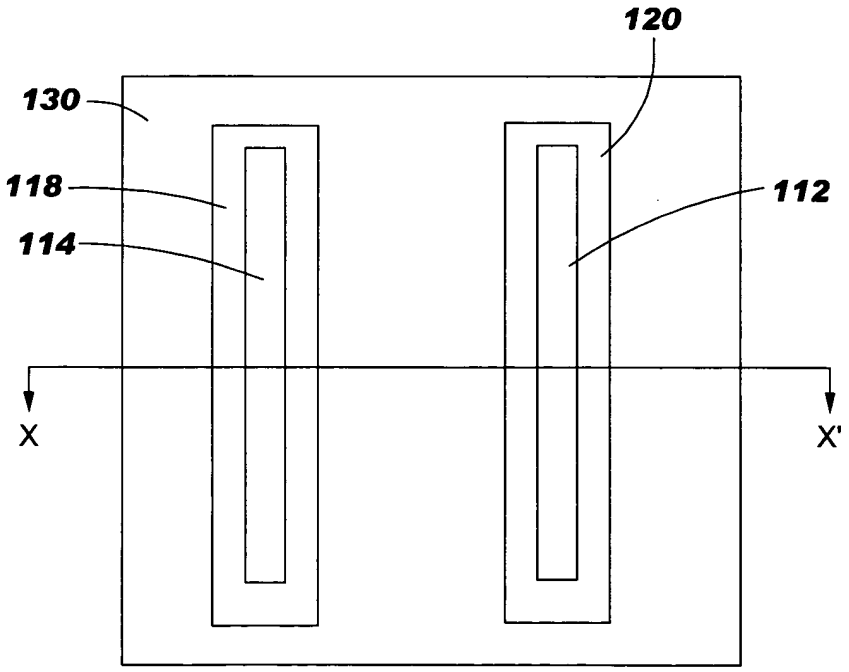


FIG. 11A

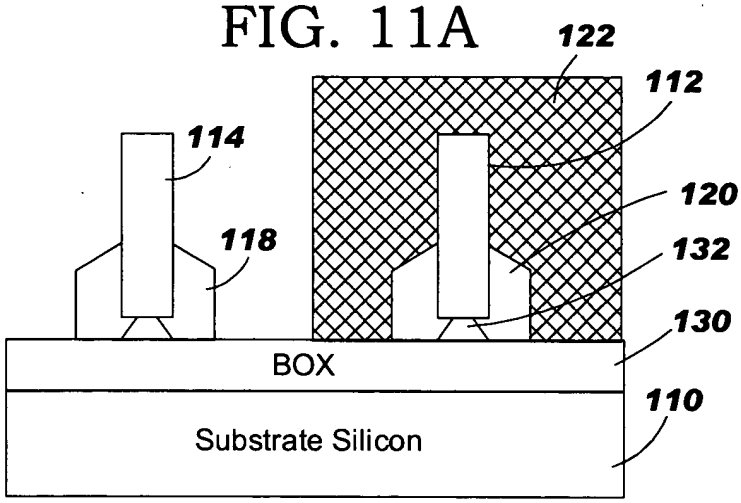


FIG. 11B

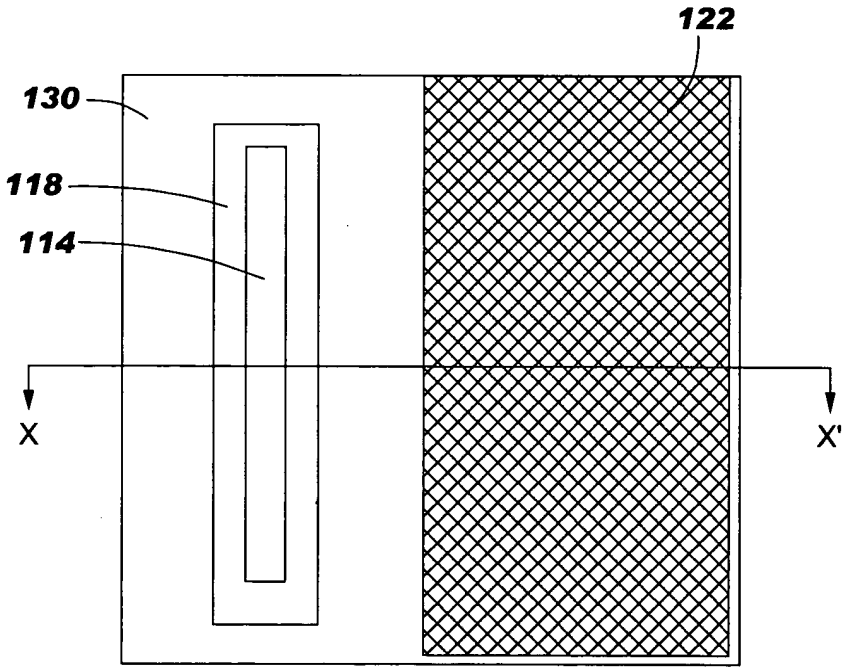


FIG. 12A

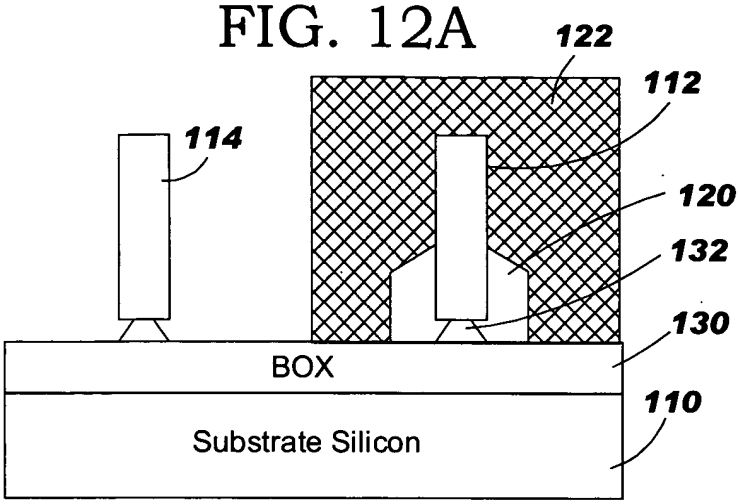


FIG. 12B

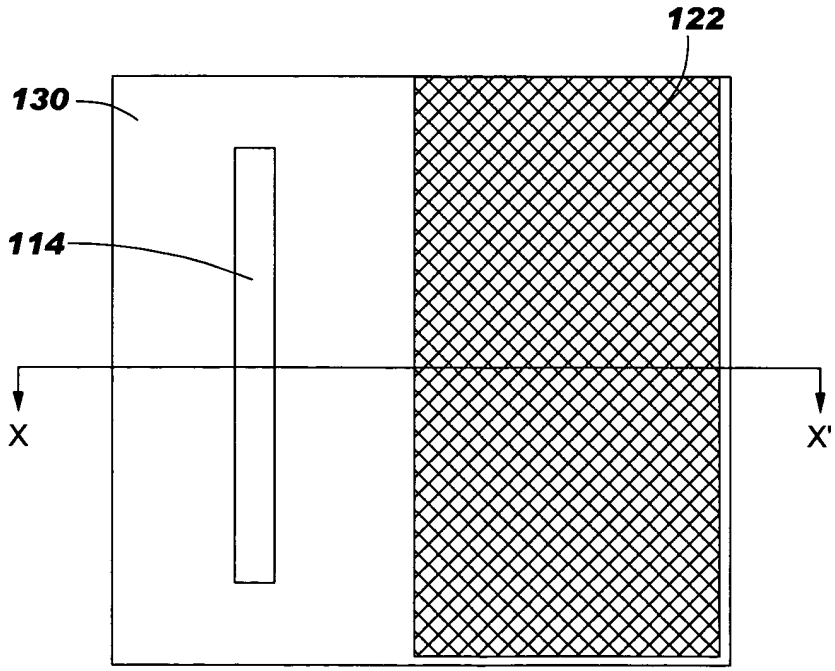


FIG. 13A

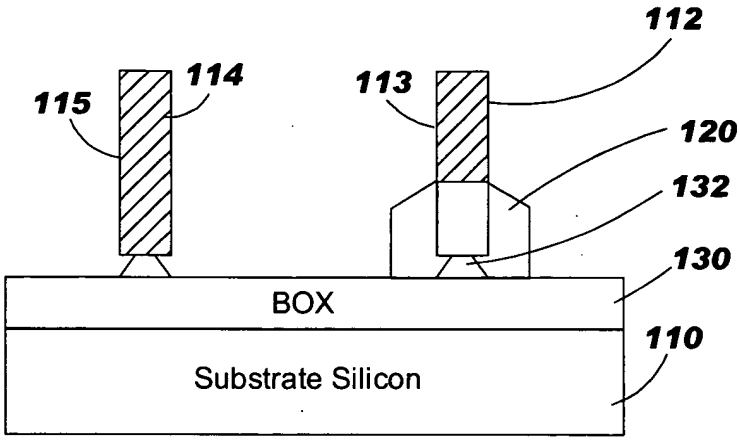


FIG. 13B

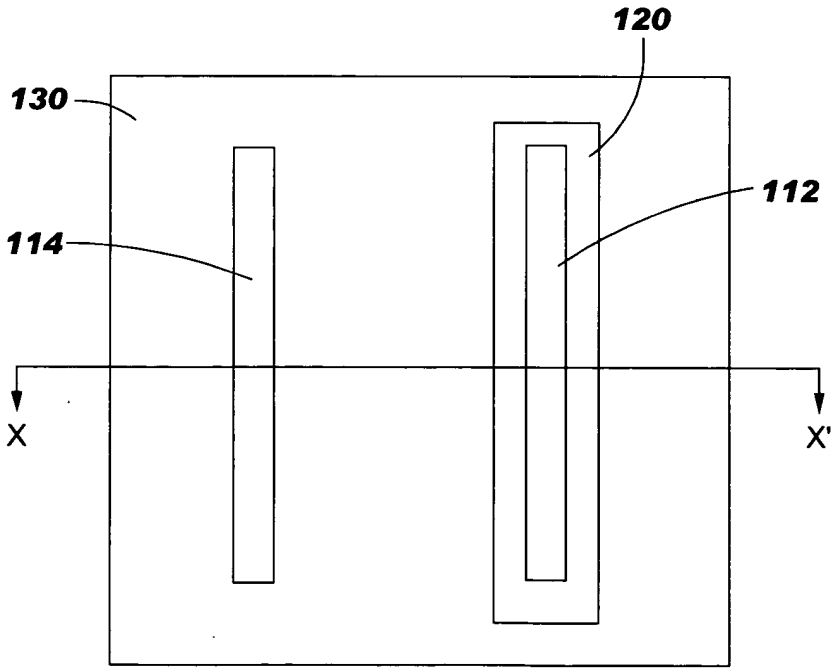


FIG. 14A

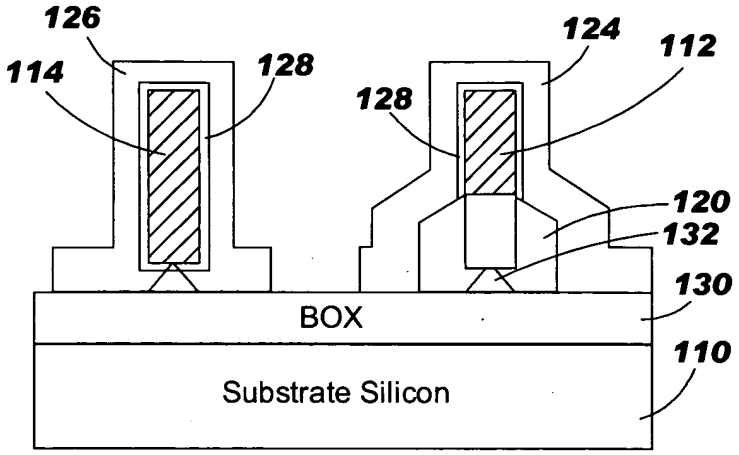
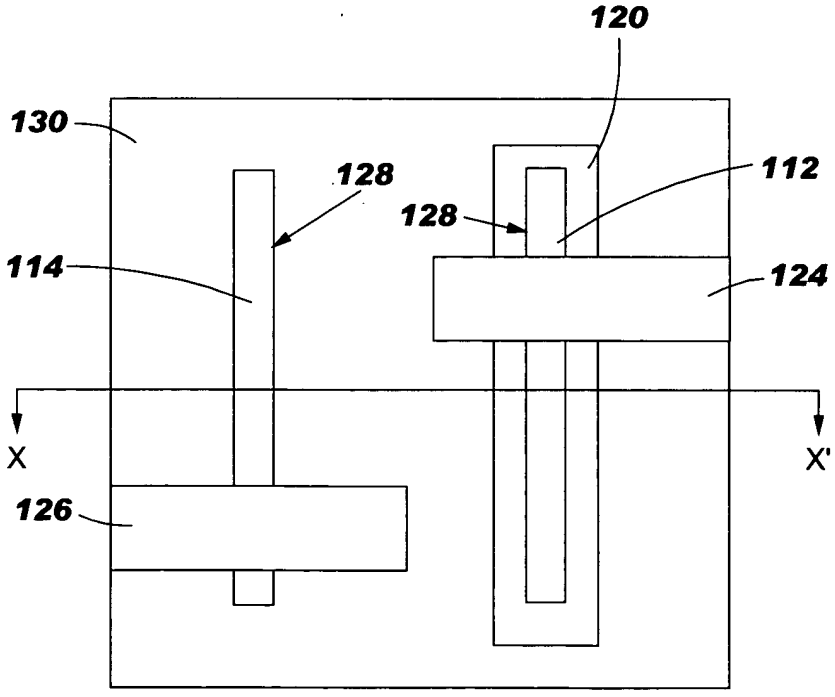
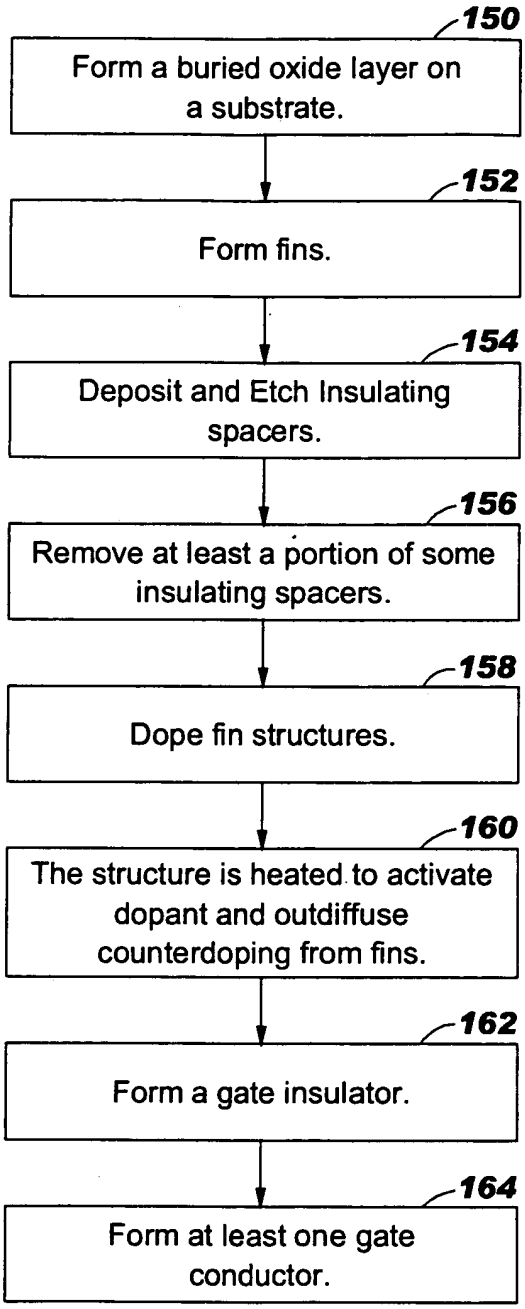


FIG. 14B



15/15

FIG. 15


150
Form a buried oxide layer on a substrate.
152
Form fins.
154
Deposit and Etch Insulating spacers.
156
Remove at least a portion of some insulating spacers.
158
Dope fin structures.
160
The structure is heated to activate dopant and outdiffuse counterdoping from fins.
162
Form a gate insulator.
164
Form at least one gate conductor.